IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#2/A
8-11-98

In re Patent Application of)
)
ELIYAHOU HARARI, ROBERT D.)
NORMAN and SANJAY MEHROTRA)
)
Serial No.: UNASSIGNED)
)
Filed: HEREWITH)
)
For: FLASH EEprom SYSTEM)
)

San Francisco, California

Assistant Commissioner of Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Please preliminarily amend the above-identified new continuation patent application being filed herewith, as follows:

IN THE SPECIFICATION:

Page 1, between lines 3 and 4, insert the following:

--Cross-Reference to Related Applications

A1 This is a continuation of patent application Serial No. 08/931,133, filed September 16, 1997, which is a continuation of 08/249,049, filed May 25, 1994, now patent no. 5,671,229, which is a continuation of application Serial No. 07/963,837, filed October 20, 1992, now abandoned, which in turn is a division of patent application serial no. 07/337,566, filed April 13, 1989, now abandoned.--

Page 11, line 26, change "Harari" to --Harari, now patent no. 5,095,344,--.

Page 11, lines 28 and 29, strike "filed on the same day as the present application," and

A2 substitute the following therefore: --Serial No. 07/337,579, filed April 13, 1989, now abandoned,--.

Page 22, line 14, insert after "204,175" --now patent no. 5,095,344,--.

Page 22, line 16, change "Techniques." to --Techniques, Serial No. 07/337,579, filed

A3 April 13, 1989, now abandoned.--

Page 26, line 3, insert a comma --,-- after "204,175" and insert thereafter --now patent

A4 no. 5,095,344,--.

Page 26, strike all of line 4, and substitute the following therefore: --Harari, Serial No.

A5 07/337,579, filed April 13, 1989, now abandoned,--.

IN THE CLAIMS:

Cancel claims 1-62, without prejudice, and substitute the following new claim therefor:

63. A flash memory card having a plurality of flash memory devices each of which is divided into a plurality or physical blocks, comprising:

a connector for connecting said flash memory card to an external device;

a data control logic circuit for controlling a transfer of data between the outside of said flash memory card and the plurality of flash memory devices through said connector and respectively transmitting block erase commands to the flash memory devices including the physical blocks to be erased when the block erase commands associated with a plurality of logic blocks are inputted via said connector; and

an address control logic circuit for managing addresses for the plurality of logic blocks inputted via said connector so as to disperse into the plurality of flash memory devices by assigning the addresses to their corresponding addresses for the physical blocks of the plurality of flash memory devices and for respectively transmitting chip enable signals to at least two device pairs of the plurality of flash memory devices including the physical blocks to be erased in such a manner that when the block erase commands are externally inputted via said connector, a period in which said at least two device pairs are simultaneously busy, exists.--

REMARKS

By this Preliminary Amendment, the original parent application claims are being canceled and a new claim 63 is being substituted therefore. This new claim is a substantial copy of claim 1 of U.S. patent no. 5,648,929 - Miyamoto et al. (1997). A copy of this patent is being filed herewith.

A prompt examination and allowance of the present application is solicited.

Dated: July 13, 1998

Respectfully submitted,

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